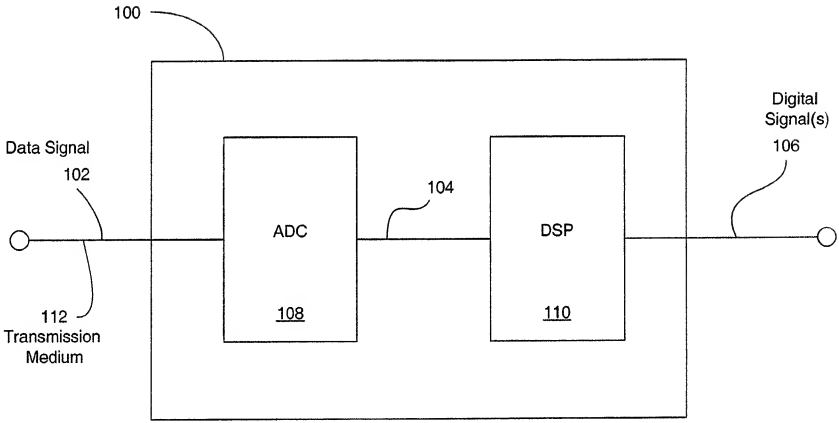


FIG. 1

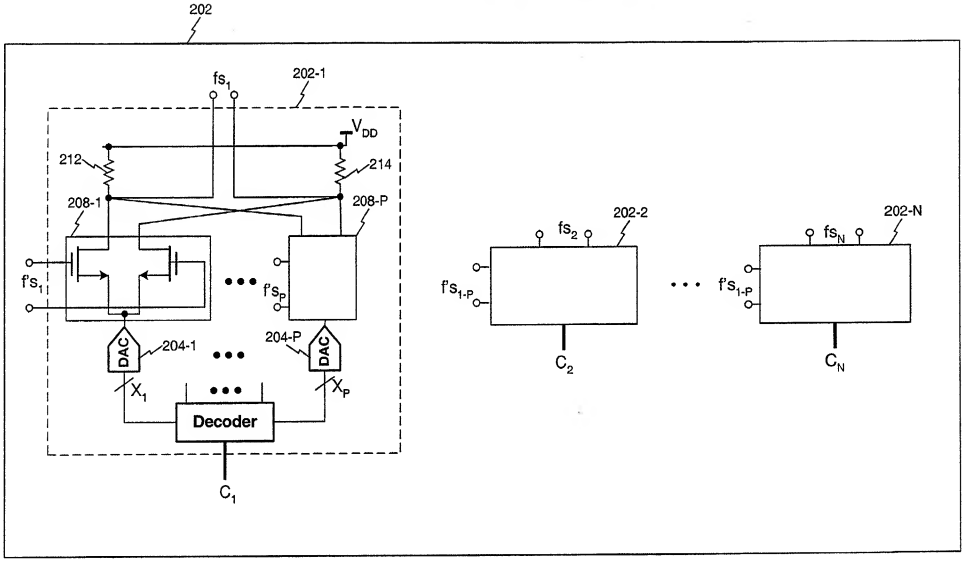
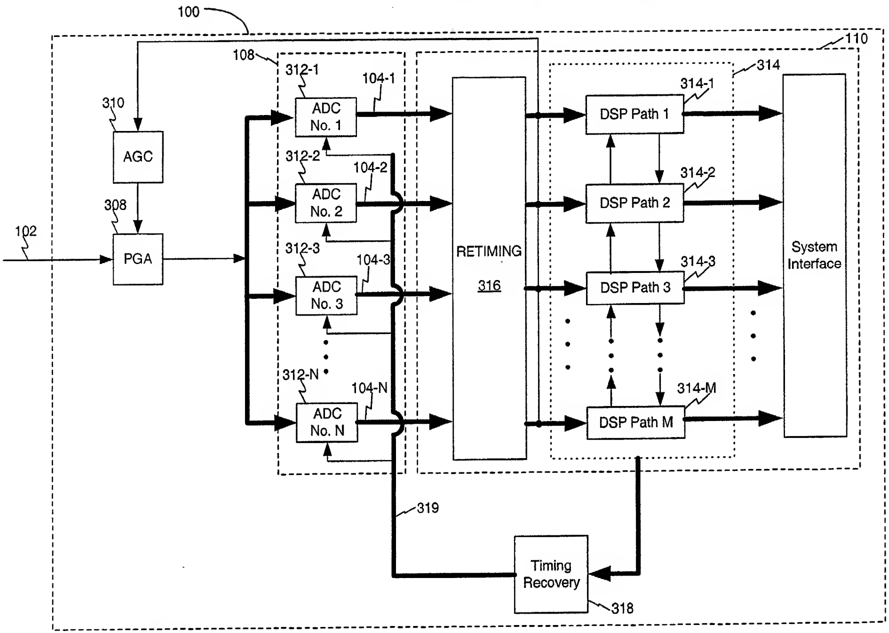


FIG. 2



100
110
108
310
AGC
308
102
PGA
312-1
ADC
No. 1
104-1
312-2
ADC
No. 2
104-2
312-3
ADC
No. 3
104-3
312-N
ADC
No. N
104-N
RETIMING
316
314
314-1
DSP Path 1
314-2
DSP Path 2
314-3
DSP Path 3
314-M
DSP Path M
System
Interface
319
Timing
Recovery
318

FIG. 3A

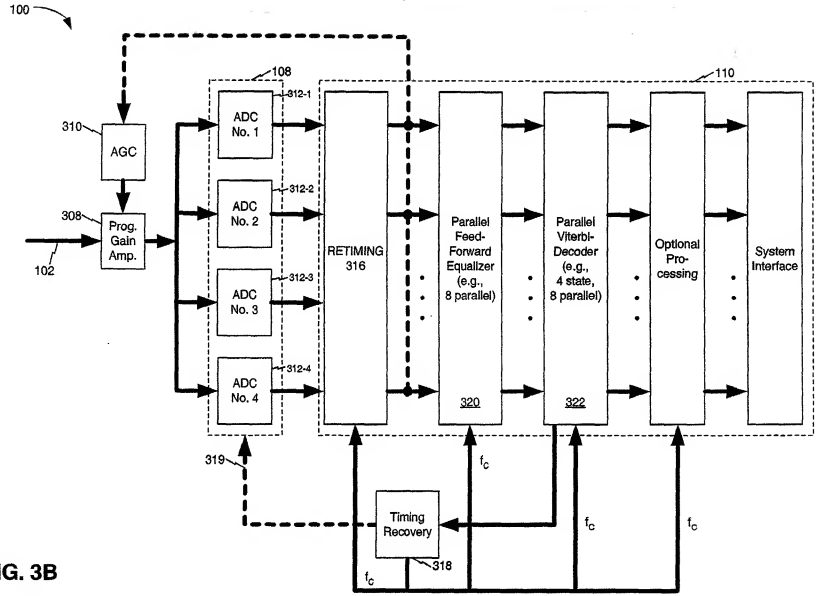


FIG. 3B

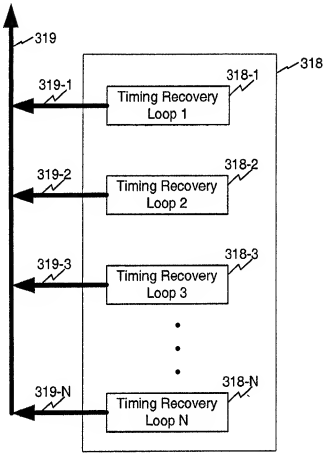

319
319-1
318-1
Timing Recovery Loop 1
318
319-2
318-2
Timing Recovery Loop 2
319-3
318-3
Timing Recovery Loop 3
319-N
318-N
Timing Recovery Loop N

FIG. 3C

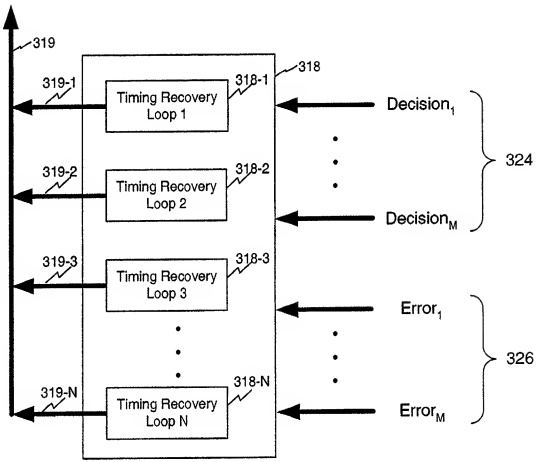

319
319-1
319-2
319-3
319-N
318
318-1
318-2
318-3
318-N
Timing Recovery Loop 1
Timing Recovery Loop 2
Timing Recovery Loop 3
Timing Recovery Loop N
Decision$_1$
Decision$_M$
324
Error$_1$
Error$_M$
326

FIG. 3D

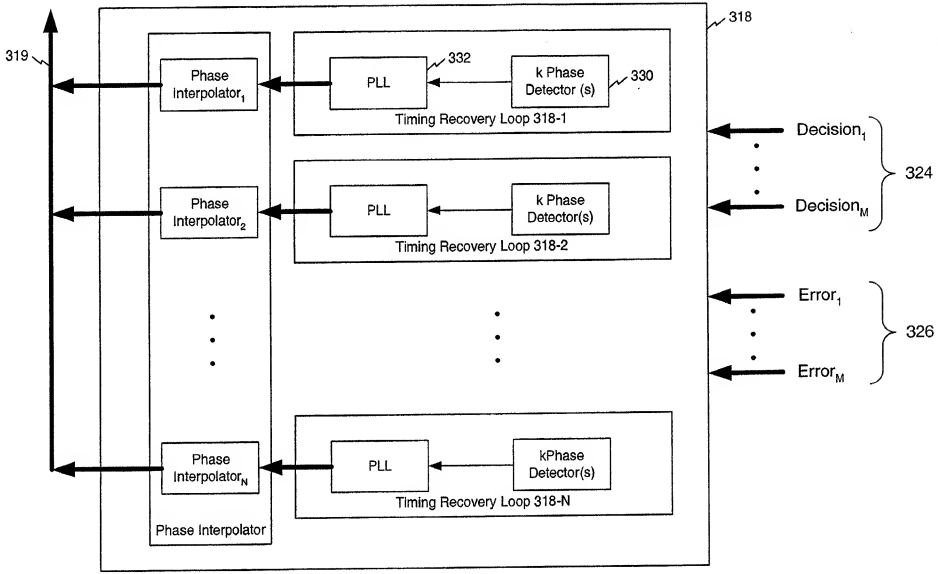

318
319
Phase Interpolator1
PLL
332
k Phase Detector (s)
330
Timing Recovery Loop 318-1
Decision1
DecisionM
324
Phase Interpolator2
PLL
k Phase Detector(s)
Timing Recovery Loop 318-2
Error1
ErrorM
326
PhaseInterpolatorN
PLL
kPhase Detector(s)
Timing Recovery Loop 318-N
Phase Interpolator

FIG. 3E

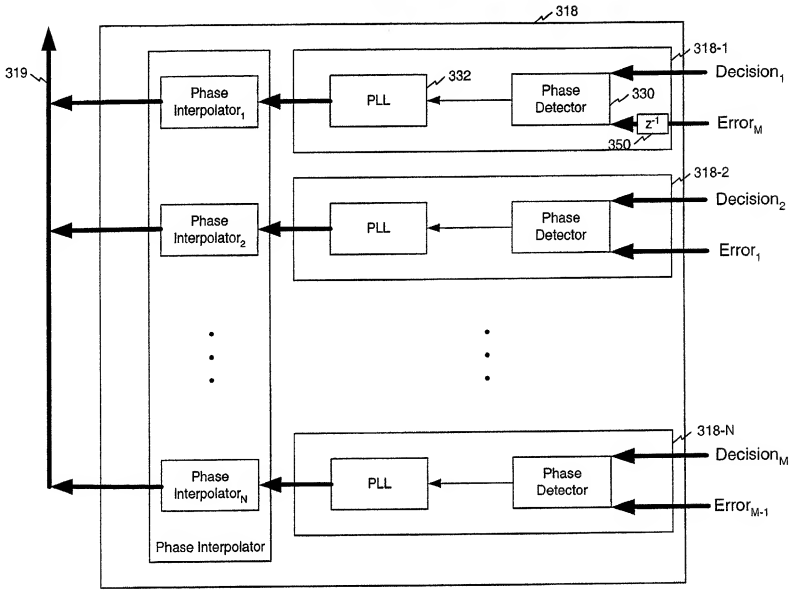


FIG. 3F

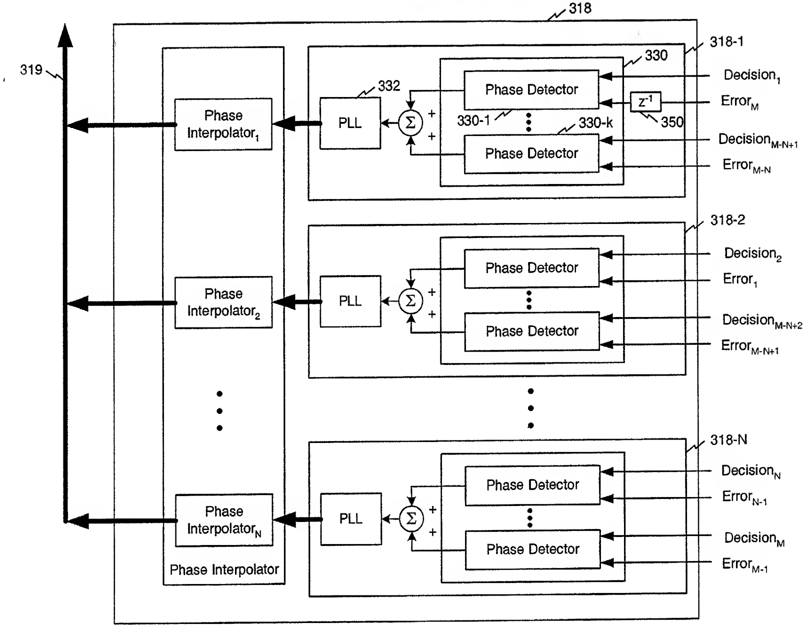

318
318-1
330
319
Decision$_1$
Error$_M$
332
Phase Detector
z^{-1}
350
330-1
330-k
PLL
Phase Interpolator$_1$
Decision$_{M-N+1}$
Error$_{M-N}$
318-2
Decision$_2$
Error$_1$
Phase Interpolator$_2$
Decision$_{M-N+2}$
Error$_{M-N+1}$
318-N
Decision$_N$
Error$_{N-1}$
Phase Interpolator$_N$
Decision$_M$
Error$_{M-1}$
Phase Interpolator

FIG. 3G

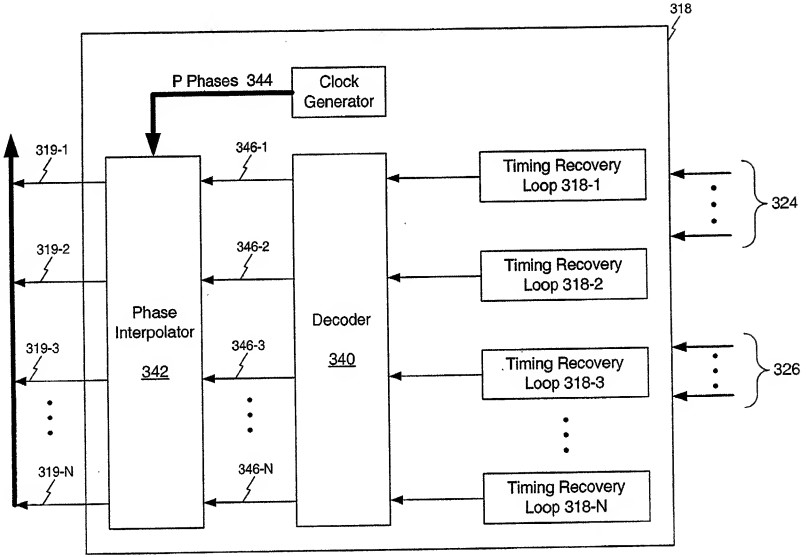

318
P Phases 344
Clock Generator
319-1
319-2
319-3
319-N
346-1
346-2
346-3
346-N
Phase Interpolator 342
Decoder 340
Timing Recovery Loop 318-1
Timing Recovery Loop 318-2
Timing Recovery Loop 318-3
Timing Recovery Loop 318-N
324
326

FIG. 3H

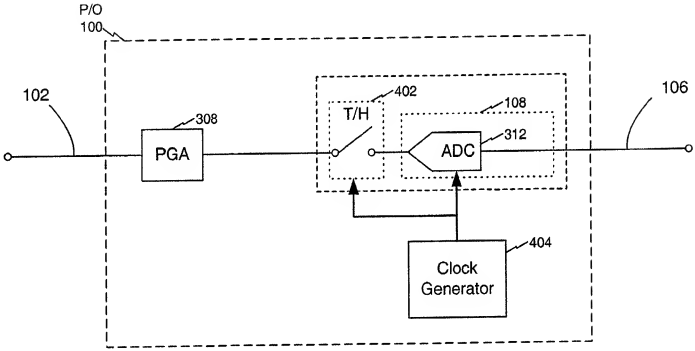


FIG. 4A

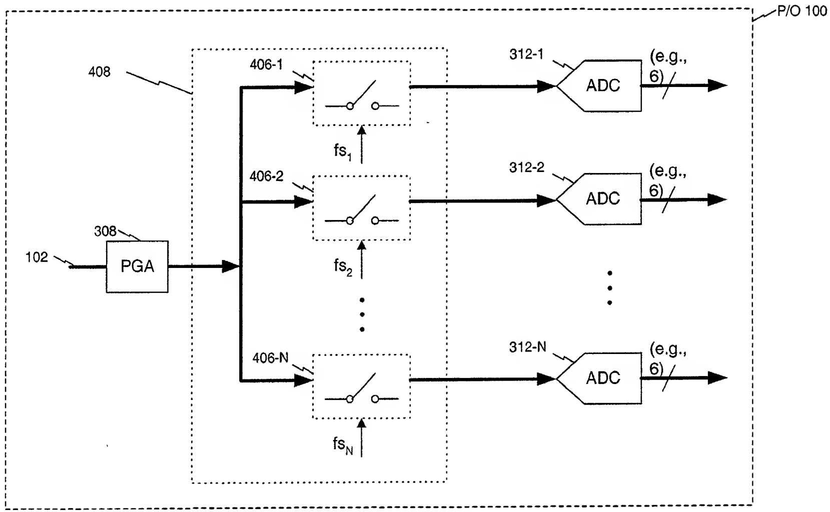

P/O 100
408
406-1
406-2
406-N
312-1
312-2
312-N
(e.g., 6)
(e.g., 6)
(e.g., 6)
ADC
ADC
ADC
fs_1
fs_2
fs_N
308
102
PGA

FIG. 4B

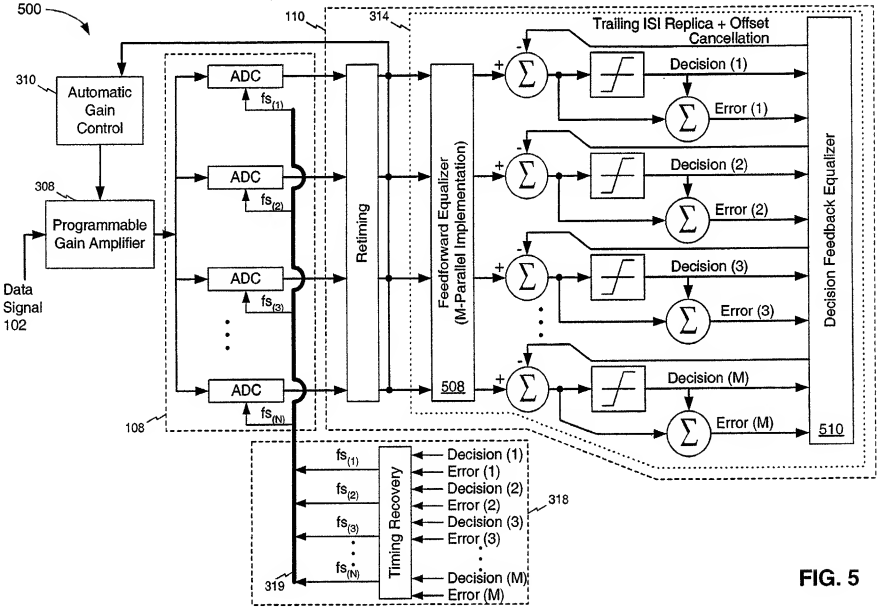


FIG. 5

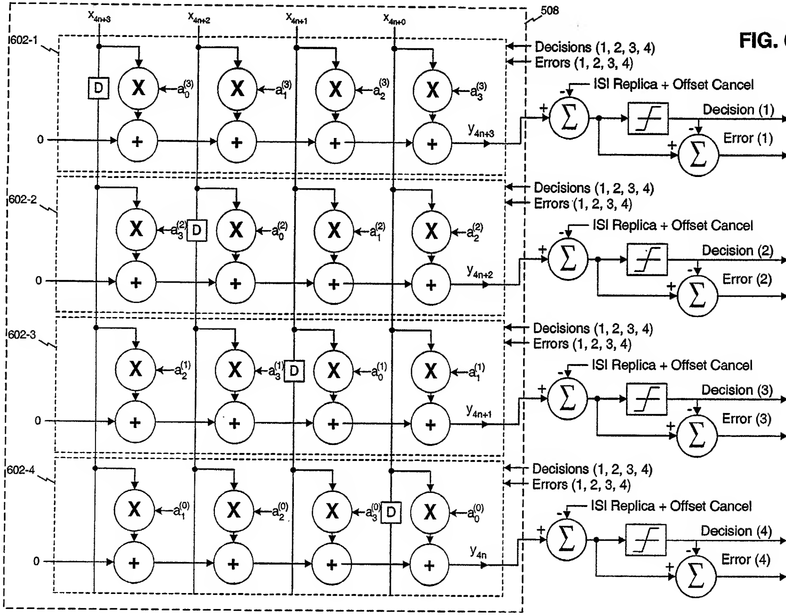

508
602-1
602-2
602-3
602-4
x_{4n+3}
x_{4n+2}
x_{4n+1}
x_{4n+0}
D
X
+
0
$a_0^{(3)}$
$a_1^{(3)}$
$a_2^{(3)}$
$a_3^{(3)}$
$a_3^{(2)}$
$a_0^{(2)}$
$a_1^{(2)}$
$a_2^{(2)}$
$a_2^{(1)}$
$a_3^{(1)}$
$a_0^{(1)}$
$a_1^{(1)}$
$a_1^{(0)}$
$a_2^{(0)}$
$a_3^{(0)}$
$a_0^{(0)}$
y_{4n+3}
y_{4n+2}
y_{4n+1}
y_{4n}
Decisions (1, 2, 3, 4)
Errors (1, 2, 3, 4)
ISI Replica + Offset Cancel
Decision (1)
Error (1)
Decision (2)
Error (2)
Decision (3)
Error (3)
Decision (4)
Error (4)

FIG. 6

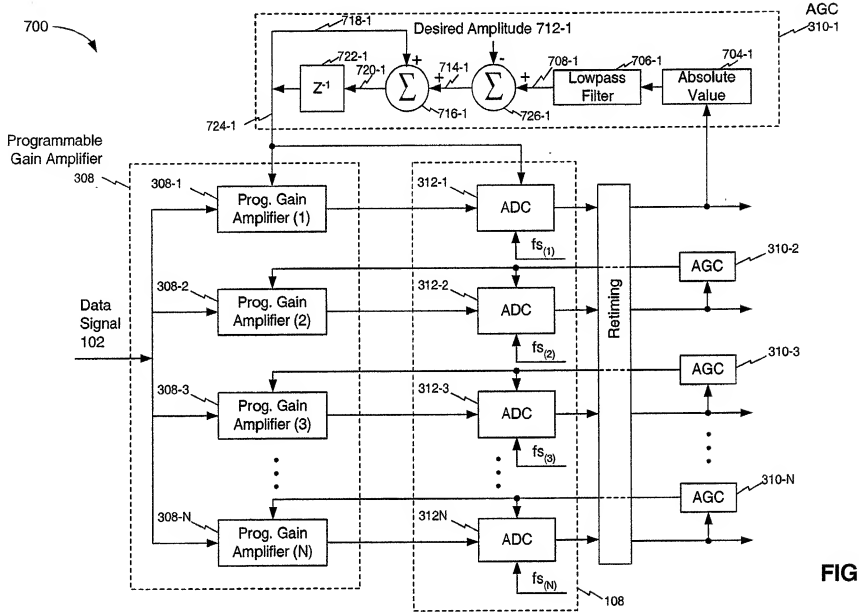


FIG. 7

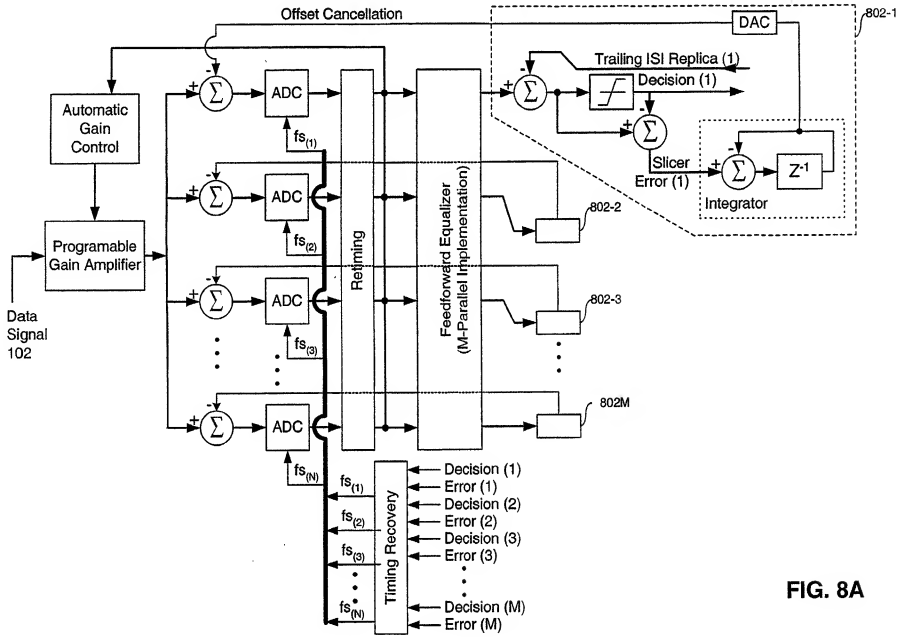


FIG. 8A

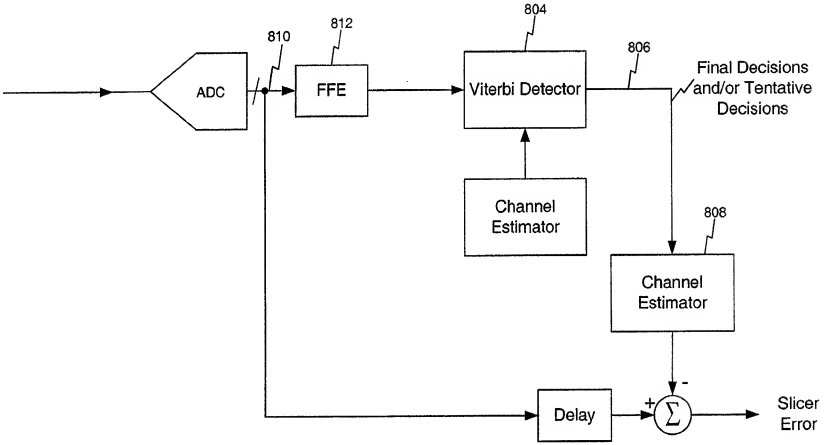


FIG. 8B

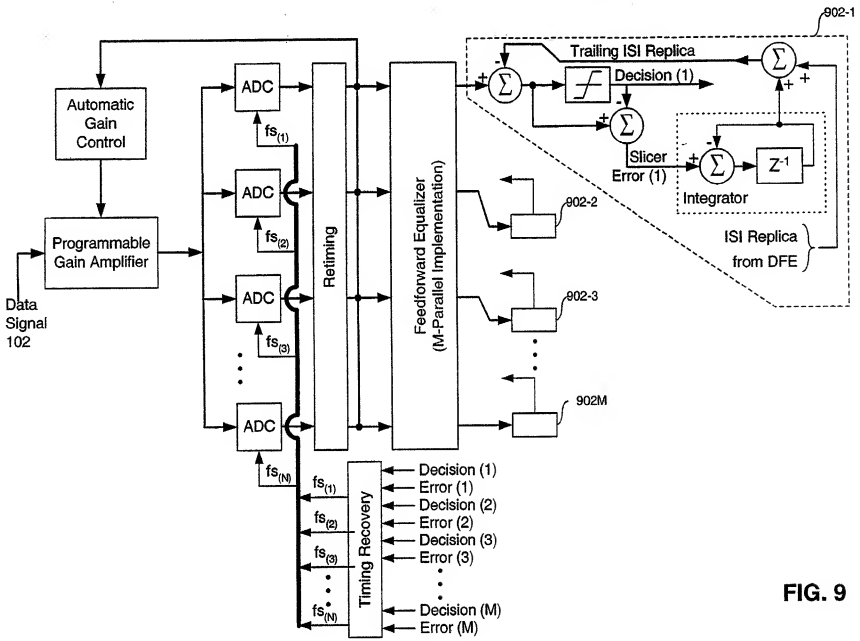


FIG. 9

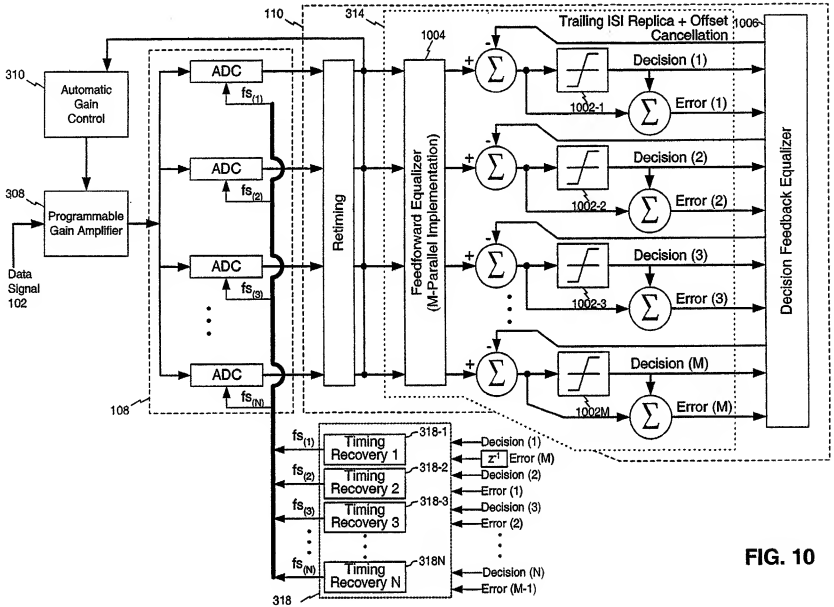


FIG. 10

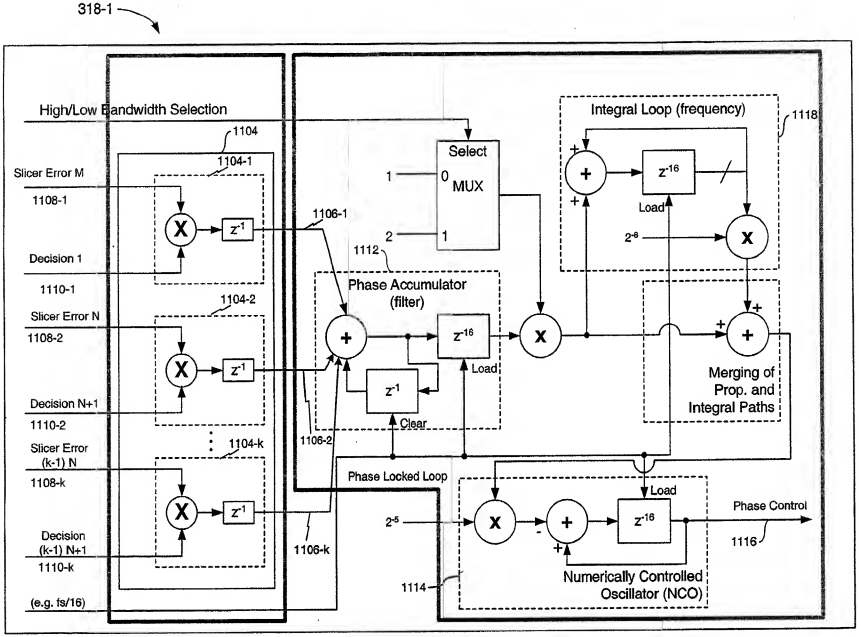


FIG. 11 Timing Recovery

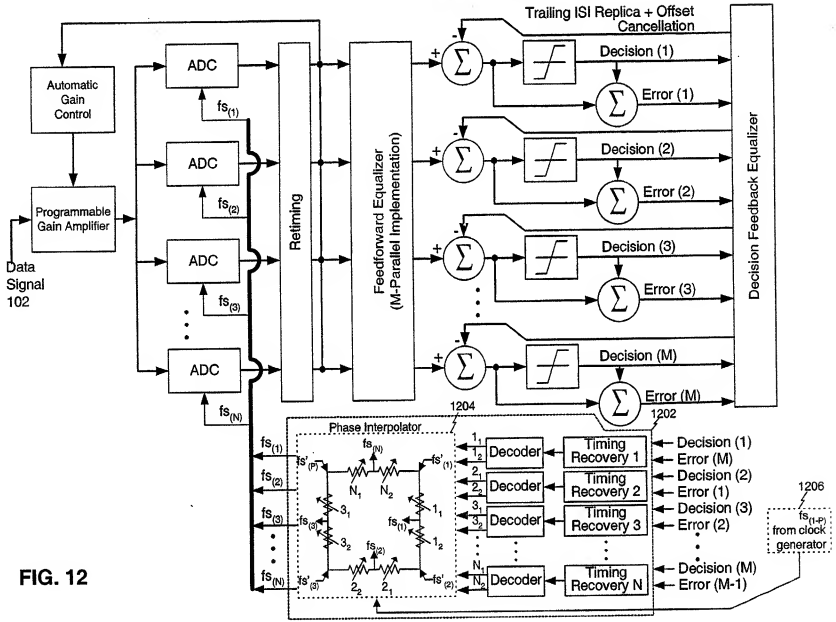
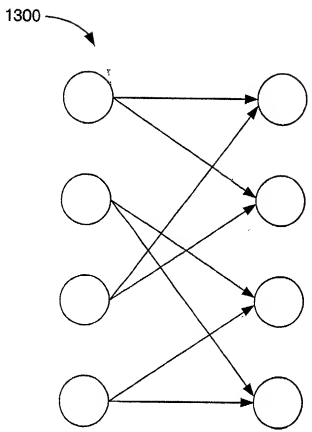
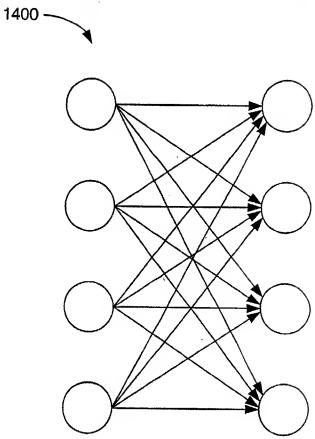


FIG. 12



4-state 1-step trellis (runs at a clock rate equal to the symbol rate)

FIG. 13



4-state M-step trellis (runs at a clock rate equal to 1/M of the symbol rate)

FIG. 14

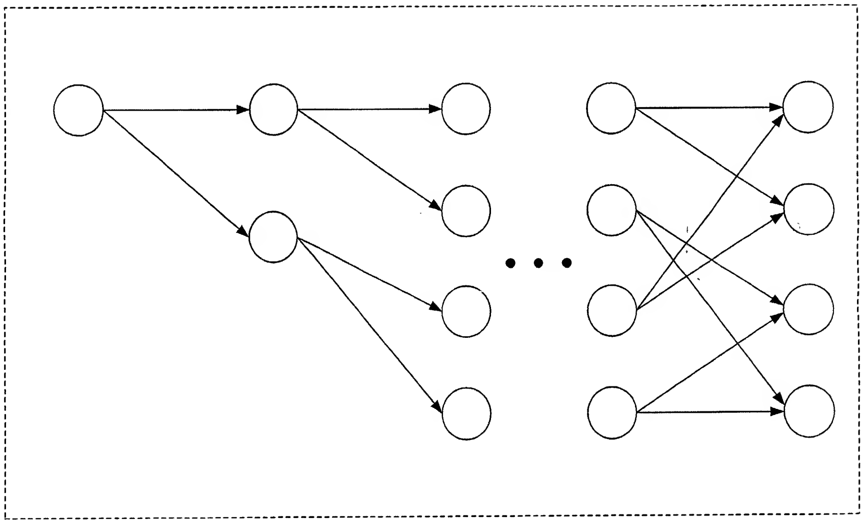


FIG. 15A

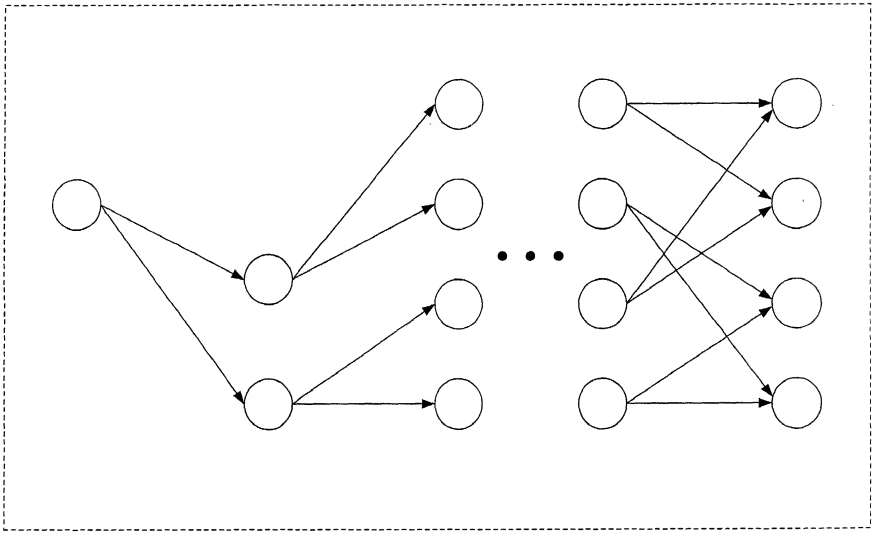


FIG. 15B

FIG. 15C

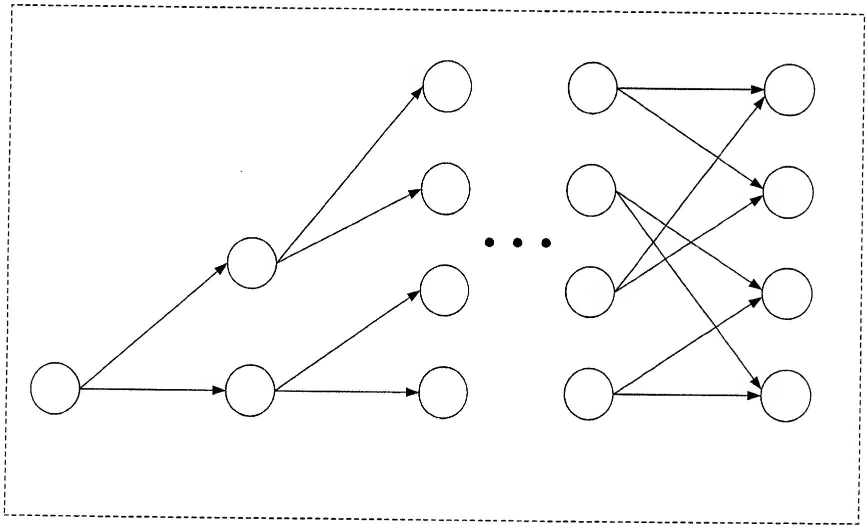
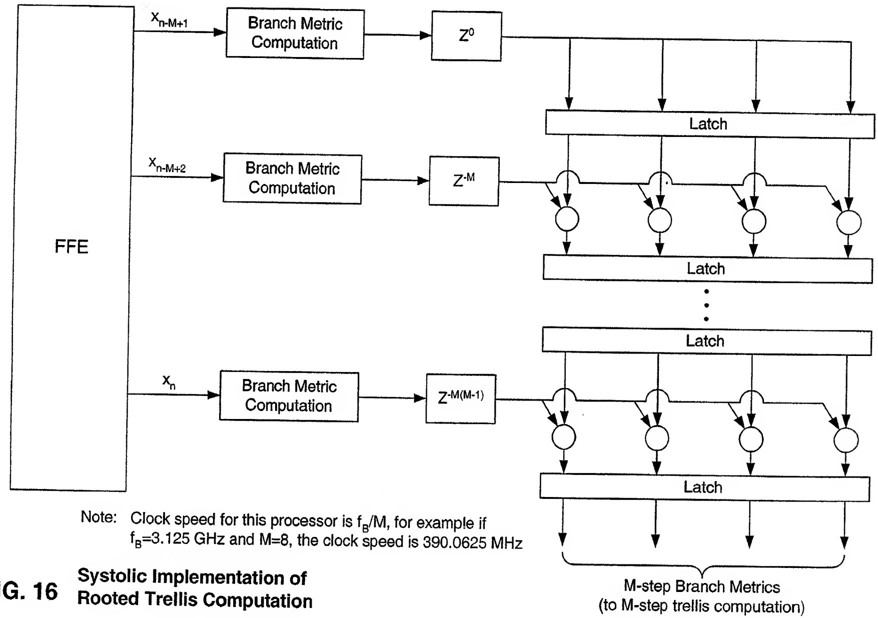


FIG. 15D



Note: Clock speed for this processor is f_B/M, for example if f_B=3.125 GHz and M=8, the clock speed is 390.0625 MHz

FIG. 16 **Systolic Implementation of Rooted Trellis Computation**

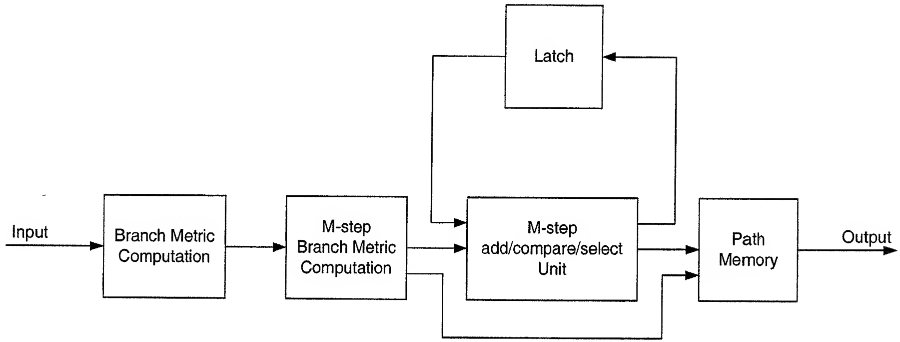


FIG. 17 **Overall Block Diagram of Parallel Viterbi Processor**

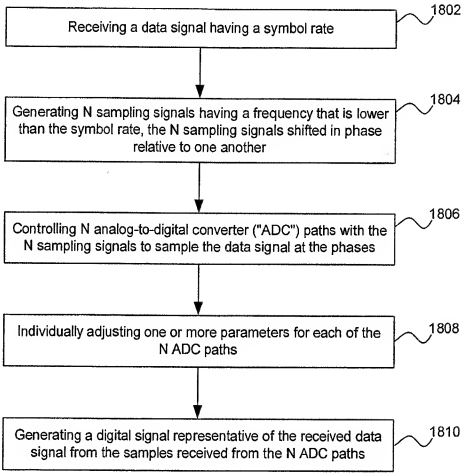

Receiving a data signal having a symbol rate
1802
Generating N sampling signals having a frequency that is lower than the symbol rate, the N sampling signals shifted in phase relative to one another
1804
Controlling N analog-to-digital converter ("ADC") paths with the N sampling signals to sample the data signal at the phases
1806
Individually adjusting one or more parameters for each of the N ADC paths
1808
Generating a digital signal representative of the received data signal from the samples received from the N ADC paths
1810

FIG. 18